

# Department of Electronics & communication Engineering

# **SANCHALANA**

E- NEWSLETTER
July 2023, Volume:8, Issue: 2

### **VISION**

Enable the students to achieve academic excellence at par with premier institutes and to meet the requirements of industry and research in the field of Electronics and Communication Engineering.

### **MISSION**

- 1. Orient the students to meet global challenges in the field of Electronics and Communication Engineering with state of-the-art facilities and excellent teachin-glearning process.
- 2. Impart knowledge in the emerging areas through industry institute-interaction, seminars, workshops and conferences.
- 3. Provide strong foundation in core subjects to enable the students for continuous learning and research.
- 4. Facilitate students for good communication, soft skills along with professional ethics.

### **Faculty Achievements:**



Dr. Mahendra H. N

Department congratulates Dr. Mahendra H. N, Assistant Professor for being awarded with PhD for the thesis titled "An Efficient Classification of Remotely Sensed data using Supervised Classifier on South – Western Part of Indian Subcontinent" by Visveswaraya Technological University, Belagavi on August 1st 2023.

❖ A MOU was signed between Department of ECE, JSS Academy of Technical Education, Bengaluru and Indian Institute of Technology, Guwahati on 12<sup>th</sup> April 2023 to encourage capacity building program for faculty, Internship, Joint Project Guidance and Student Development Programs



### Student achievements:

Final year students Sahana A R , Gowtham Suresh and Chirag V of ECE Department participated in National level hardware hackathon organized by IEEE India Council in collaboration with CDAC - Thiruvananthapuram and was held during the IEEE Guwahati Subsection Conference (GCON-2023) at Indian Institute of Technology, Guwahati from 23 to 25 June, 2023. They presented a snake robot titled "RAPTOR - Robust Articulated Platform for Terrain Observation and Rescue". The robot was constructed using India's Indigenous VEGA Processor. They had designed and 3D printed each articulating component and integrated them with the electronics. The versatile robot is capable of traversing various terrains, and has the added flexibility of interfacing sensors and actuators.



Three student papers were presented on 23<sup>rd</sup> June 2023 in the "IEEE GCcon 2023" at Indian Institute of Technology Guwahati under the guidance of Dr. Thejaswini P.

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Name of the Project
Application of Error Detection and
Correction Techniques to Self-Checking

VLSI Systems: An Overview

Sahana A R , Gowtham S, Chirag V

Secure Video Streaming Techniques: A Performance Overview



Sagar Dev Achar, Shankar Singh C



Reverse Engineering techniques for Android systems: A Systematic approach

\*\* 8th Harshitha semester students R(1JS19EC053), Ajay Vardhan V (1JS19EC011), P(1JS19EC015), Amrutha Н Darshan S(1JS19EC036) participated in "Kaushalya" Open House Project Expo-2023, IEEE YESIST12 2023 Prelims at NITTE Meenakshi Institute of Technology, Bengaluru on 4th May 2023 and awarded as the BEST PROJECT for "Classification of VPK Using Facial Recognition" under the guidance Mr.Suguna G C.



Three student project batches have been sanctioned with Rs. 5000/- from Kranataka State Council for Science and Technology (KSCST).

Name of the Student	Name of the Project
Sudarshan E	Design And Development of
Raghunandan V	Noninvasive Medical Device for
Vaishnavi P	Health Monitoring Using Ppg
Spoorthy R	Signal
Guide: Dr. Veerabhadrappa S T	
Chethan S	E-Health Monitoring and
Kruthika B	Medicine Prescription
Managoli Muktha S	Generation System Using lot
Jitendra S H	and Machine Learning
Guide: Mr. Mahendra H N & Dr. Mallikarjunaswamy S	
Likhita B Patil	
Adithya A	Dol-Skindi (Detection of Lumpy
Anusha M	Skin Disease)
Manjunatha G C	
Guide: Dr. P M Shivkumaraswamy & Manohar B S	

### **Department Activities:**



Importance of Up skilling and Entrepreneurship

❖ Technical talk on "Importance of Up skilling and Entrepreneurship" was conducted on 11th February 2023. The resource person was Mr. T S Sarang, Co-founder, M/S Inovact Private Ltd. Total of 125 students of 1st year attended the talk. Workshop Cloud Computing on was conducted association with in M/s Foundation for Innovation and Collaborative Education (FICE), VOIS (Vodafone Intelligent Solutions), from 02nd to 4th March 2023. The resource person was Mr. Ankur Sharma, Master trainer, FICE. Total of 137 students of 3rd semester attended the workshop.



- A Technical talk on "Applications of IoT" conducted on 22nd February 2023for 1st year students. Mr.Karthikeyan S, Technical head @ IObit Solutions was a speaker for the talk. Total of 158 students of attended the workshop.
  - Two days hands on workshop on "Hardware Security and Logic Locking" was organized from 2nd to 3rd June 2023 in association with IETE student chapter. The resource person was Mr. Vivekananda G, Research scholar, IIT Guwhati. Total of 40 students of 6th sem attended the workshop.



Hardware Security and Logic Locking

- A Workshop on "MATLAB" was conducted on 17th May 2023.Mr.Niveitha Mohan kumar, Education Customer Success Specialist, Mathworks, Mr. Avinash, Application Engineer, Core El Technologies Were the resource person for the workshop.
- ❖ A Technical talk on "The Blueprint for Success: Strategies for Career and **Placement** Development Opportunities" was conducted on 12th 2023.Mr. April Ajay Murdeshwar, Performance Marketing expert, Career Labs Technologies was a resource person for the event. A total of 80 students attended the talk.



The Blueprint for Success: Strategies for Career Development and Placement Opportunities

One day workshop on PCB Design was conducted on 21st February 2023 for 3rd and 5th semester students. The resorce person for the event was Mr. T S Sarang, Co-founder, M/s Inovact Private Limited. Total of 136 participated in the event.





"MATLAB Workshop" for the 4th semester students was organized on 24th July 2023. The training Course provides a platform for the students to develop their skills using MATLAB through various tool boxes available in MATLAB. The resource person for the workshop was. Mr. Avinash Vulasa, Application **Engineer-UPT** Technology Solutions Division, CoreEL Technologies. 165 students attended the workshop.

### Parent Teacher Meeting:

Parent Teacher Meeting was conducted to discuss about the department progress, Activities conducted for students, Student Performance and attendance in their internal assessment and Placement Activities.

Link: https://meet.google.com/gio-tqwp-noc



### **Editorial Board**

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# Department of Electronics & communication Engineering

# **SANCHALANA**

E- NEWSLETTER
January 2023, Volume:8, Issue: 1

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### **Faculty achievements**



Dr. Savitha A C

• Dr. Savitha A C, Assistant Professor has been awarded with PhD for the thesis titled "Development of secured Energy Efficient Algorithm for Machine to Machine Communication Using LTE Networks" by JSS Science & Technology, Mysuru on 22<sup>nd</sup> December 2022.



Dr. Sangeetha K N

- Dr. Sangeetha K N, Assistant Professor has been awarded with PhD for the thesis titled "Cognitive Based Data Classification And Image Steganographic Algorithm Using Selection Artificial Intelligence Techniques" Visveswaraya Technological University.
- Department congratulates **Mr.** Srikantaswamy S C for his promotion as Foreman and getting transferred to EI department on 21<sup>st</sup> march 2023.

### **MOU** signed

❖ A Memorandum of understanding was signed between Department of Electronics & Communication Engineering and Centre for Development of Advanced Computing C-DAC (T), Vellayambalam, Thiruvananthapuram on 19<sup>th</sup> December 2022.





❖ A Memorandum of understanding was signed between Department of Electronics & Communication Engineering and M/s Inovact Private Limited, #731, E & amp; F Block, Kuvempunagar, Mysore-570023, on 22<sup>nd</sup> December 2022.

### **Department Activities**



India's Indigenous Microcontroller Development Board VEGA Processor and Ecosystem

❖ A Special Lecture & live demo on HAM radio system was organized for 3<sup>rd</sup> semester students on 26<sup>th</sup> November 2022. The resource person for the program was Mr. Abhishek and team from Gravity Science foundation, Mysuru Total of 60 students attended the program.

Department of Electronics & Communication organized two days national level hands-on workshop on "India's Indigenous Microcontroller Development Board VEGA Processor and Ecosystem" in collaboration with C-DAC and IEEE India Council on 20th and 21st of October, 2022 proliferate "VEGA processors" series microprocessors including India's first indigenous 64-bit multi-core RISC-V based Superscalar Out-of-order Processor among the academic community. This is the first Pan India workshop on indigenous VEGA Processors for students of 2<sup>nd</sup> and 3<sup>rd</sup> year students. The chief guest for the workshop is Mr. Libin T T, Scientist F, C-DAC, Thrivandrum. The guest of honor is Dr. Dr. H R Mahadevaswamy, Joint Director, Technical Division, JSSMVP. The workshop provides a platform for the



HAM radio system

NASA International Space Apps Challenge "Ideathon 2022" was held in association with NASA on 15<sup>th</sup> & 16<sup>th</sup> December 2022.Ms. PoojaTak, Co-Founder, Pravishya Tech, Mumbai & NASA Apps, Karnataka State Lead, Mr. Sandeep Ravikanti, Co-founder, Trivent Technology, Hyderabad were present during the event. Total of 92 teams participated in the event.



❖ A Technical talk on "Carrier Opportunities in Core Companies" was conducted on 23<sup>rd</sup> December 2022 for 5<sup>th</sup> semester students. Mr. Abhilash Krishna, Physical Design CAD Engineer was a speaker for the talk. Total of 54 students participated in the event.



projects and Solutions" is organized for students of 3rd semester from 18th to 20th October 2022. The resource persons were Mr .Mohan Shamanna , Founder and Mentor , M/s Indoskill, Bengaluru, Mr. Mohammed Azhar Hussain, Co-Founder and Mentor , M/s Indoskill, Bengaluru, Mr. Madhu N, Data Analyst, M/s Techno Genesys, Bengaluru, Mr. Ramakrishna G, Data Analyst, M/s Techno Genesys, Bengaluru, Mr .Yashwanth Kaushik, Data Analyst,

M/s Techno Genesys, Bengaluru. Total of 180

students attended the program.

A workshop on "Python Coding with application



Chief Guest addressing the participants



Carrier Opportunities in Core Companies

One day workshop on PCB Design was conducted on 17<sup>th</sup>October 2022 for 3<sup>rd</sup> and 5<sup>th</sup> semester students. The resource person for the event was Mr. T S Sarang, Co-founder, M/s Inovact Private Limited. Total of 130 students participated in the event.



Python Coding with application projects and Solutions

### **Student Achievements**

❖ 2 teams each from ECE department have bagged a prize of Rs. 2,00,000 /- in "Tech Innovation Marathon", Showcase Event of \_VOIS for Tech Innovation Marathon 2022 from July 2022 to October 2022 held in Pune. Team members are Vijay M, Sumukh A, Tushar M S, Tarun G V, Shankar Singh C, Sumanth Rao CS from 7th semester.



Tech Innovation Marathon

### **Industry visits**

❖ 9 faculty members of Department of Electronics & Communication Engineering visited Tessolve Semiconductor Private Limited, Electronic city, Bengaluru, Karnataka on 10<sup>th</sup> December 2022.



United Telecoms Ltd. Goa broad band network



❖ As part of the engineering curriculum, the 7<sup>th</sup> semester students, Electronics & Communication Department visited the United Telecoms Ltd. Goa broad band network, Goa from 2<sup>nd</sup> December 2022 to 4<sup>th</sup> Dec 2022. Total of 68 students participated in the industry visit and gained firsthand information on industry development.

### **Student Articles:**

### Need for Logic Locking in hardware security

Ever-increasing design complexity and the skyrocketing cost of setting up a foundry have led to globalization of integrated circuit (IC) supply chain. A globalized and distributed IC supply fosters security threats such as reverse engineering, piracy, and hardware Trojans, and forces the stakeholders to revisit the trust at various steps in the IC design and fabrication flow. Among the ensemble of solutions proposed to address hardware related trust issues, logic locking has gained significant interest from the research community. A series of defense techniques and attacks have been developed over the past few years.

Integrated circuits (ICs) are ubiquitous and an essential component of electronic systems ranging from home appliances and smart phones to satellites and military equipment. ICs serve as the root-of-trust for computing systems. The software computations can only be trustworthy if the underlying hardware is reliable and trust worthy. IC supply chain has evolved drastically over the years. Traditionally, companies such as Intel and IBM would use to foundries, and design and fabricate ICs in-house, in trusted settings. However, the evolving complexity of integrated circuits (ICs), the ever-shrinking time-to-market, and the skyrocketing costs of building or maintaining a semiconductor foundry have propelled the globalization of IC design and manufacturing flow.

As of today, many semiconductor companies, such as Apple, operate fabless and outsource the fabrication of ICs to offshore foundries. Apart from the fabrication of ICs, test, assembly, and packaging services may also be outsourced to outsourced assembly and test (OSAT) companies such as ASE [27] and Amkor [2]. Even design houses may purchase and use third-party intellectual property (3PIP) cores to reduce their design effort and meet strict time-to-market constraints. In a globalized and distributed IC supply chain, several (potentially untrusted) agents have access to the valuable IP or the physical IC. This increased access to critical assets opens up opportunities for rogue elements to exploit valuable information and/or jeopardize the trust in the IC design flow. Hardware security vulnerabilities and threats that have emerged at various stages of the IC supply chain, as a consequence of the globalization, are highlighted in Figure below.



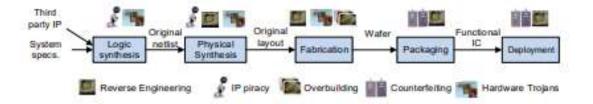
Ms.Lakshmi Manoj 1JS20EC040



Mr.Nikhil Thevas 1JS20EC052



Ms.Sanjana James 1JS20EC076



The security threats at different stages in the IC design flow. A rise in the number and devastating capability of hardware-based assaults has brought attention to the necessity of protecting the hardware root of trust alongside improvements in power, cost, performance and reliability. The whole design of an integrated circuit can be concealed from a suspect foundry or end-user via a key-based circuit obfuscation or logic-locking approach. The method is based on introducing "key" input bits into the circuit to introduce ambiguity within the original circuit, rendering the circuit unreadable without the proper secret key. The present level of knowlwdge in this developing area is limited and includes a threat model classification such as hardware Trojans, reverse engineering (RE) and side channel analysis.

### **Editorial Board**

### **Staff Coordinators:**

- Dr. P M Shivakumarswamy, HOD
- \* Mrs. Sunita Shirahatti, Asst. Prof.
- Mrs. Asharani, Instructor

### **Student Coordinator:**

Ms.Lakshmi Manoj, 6<sup>th</sup> Sem

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